Abstract of the Disclosure

In a shift and shift-out detecting circuit, a plurality of partial shift circuits respectively have bit shift quantities which are different from each other, and are connected in series. Each of the plurality of partial shift circuits receives a shift result as a previous shift result from the partial shift circuit of a previous stage and a corresponding shift instruction, shifts the previous shift result by the corresponding bit shift quantity in response to the shift instruction to produce a current shift result, and outputs the current shift result to the partial shift circuit of a subsequent stage. A plurality of shift-out detecting circuits are respectively provided for the plurality of partial shift circuits. Each of the plurality of shift-out detecting circuits detects a shift-out of "1" bit from the current shift result and the corresponding shift instruction and generates a partial sticky signal when the shift-out is detected. A collecting circuit collects the partial sticky signals from the plurality of shift-out detecting circuits and generates a sticky signal to indicate generation of the shift-out.